K16U 2070

Reg. No. : .....

Name : .....

III Semester B.C.A. Degree (CBCSS – Reg./Supple./Improve.)
Examination, November 2016
(2014 Admn. Onwards)
Core Course
3B06 BCA : COMPUTER ORGANIZATION

Time : 3 Hours Max. Marks : 40

SECTION – A

1. Fill in the blanks : **(8×½=4)**

   a) Each pipeline stage is expected to complete in _____ clock cycle.

   b) The potential increase in performance resulting from pipelining is proportional to the number of _____

   c) Each memory cell can hold _____ bit of information.

   d) Memory cells are organized in the form of _____

   e) One row is one memory _____

   f) Two transistor inverters are cross connected to implement a basic.

   g) Memory bandwidth is the number of _____ or _____ that can be transferred in one second.

   h) _____ can transfer a block of data from an external device to the processor, without any intervention from the processor.

P.T.O.

SECTION – B

Write short notes on **any seven** of the following questions. **(7×2=14)**

2. What is the significance of addressing mode ? Explain any one addressing mode.
3. What is arithmetic overflow ?
4. Explain straight-line sequencing of instruction execution.
5. Explain Three-state bus buffers.
6. Explain different instruction code formats.
7. What is interrupt service routine ?
8. What is control memory ?
9. What is programmed I/O ?
10. What is hit ratio ?
11. What is an effective address ?

SECTION – C

Answer **any four** of the following questions. **(4×3=12)**

12. Explain instruction cycle.
13. Describe the general register organization of CPU.
14. Explain priority interrupt.
15. What is locality of reference ?
16. Distinguish between RISC and CISC.
17. Explain 2's complement addition with an example.

SECTION – D

Write an essay on **any two** of the following questions. **(2×5=10)**

18. With the help of a diagram explain Set Associative Memory mapping.
19. Explain Microprogrammed Control Unit.
20. Explain pipelining in detail.
21. Give an account of stack organization.