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III Semester BCA Degree (CBCSS-Reg./Sup./Imp.) Examination, November - 2019 (2014 Admn. Onwards) CORE COURSE 3B07 BCA:INTRODUCTION TO MICROPROCESSORS

Time : 3 Hours

Max. Marks: 40

Section-A

1. One Word Answer

(8×0.5=4)

- a) The number of address lines of 8085 is _____.
- b) A 20-bit address bus can locate _____ locations.
- c) NMI stands for ______
- d) The contents of accumulator before CMA instruction are A5H. Its content after instruction execution is _____
- e) AAM instruction is used for _____.
- f) Status register is also called as ______
- g) In cascaded mode, the number of vectored interrupts provided by 8259A is _____.
- All the functions of the ports of 8255 are achieved by programming the bits of an internal register called _____.

Section-B

Write short notes on any Seven of the following questions. (7×2=14)

- 2. What type of architecture is used in 8085.
- 3. What is the difference between primary and secondary storage device?
- 4. Explain how pipelined architecture is implemented in 8086.
- 5. Explain the instructions related to interrupt subroutines.
- 6. What is queue. How queue is implemented in 8086.

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- 7. What is SIM and RIM instructions?
- 8. What is the difference between DW and DD directives?
- 9. What is the difference between respective shift and rotate instruction?
- 10. What are the features of mode 0 operation in 8255.
- 11. What is Cycle Stealing?

Section-C

Write short notes on any Four of the following questions. (4x3=12)

- 12. Explain the addressing modes of 8086.
- 13. Describe execution of a CALL instruction.
- 14. Explain four flag manipulation instructions in 8086.
- Compare maskable and nonmaskable interrupts.
- 16. How does the DMA controller 8257 perform direct memory access?
- 17. What is handshaking port? Explain the working of this port.

Section-D

Write short notes on any two of the following questions.

 $(2 \times 5 = 10)$

- 18. Draw and explain the architecture of 8086.
- 19. Differentiate minimum mode and maximum mode of 8086 with diagram.
- 20. Explain the interrupt response sequence of 8086.
- 21. Explain Programmable Peripheral Interface with block diagram.